AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (original): A damascene gate process, comprising:

providing a semiconductor substrate having a pad layer and a etch stop layer formed thereon;

forming an insulating layer to cover the etch stop layer;

forming an opening be partially removing the insulating layer, the etch stop layer, and the pad layer;

forming a protective spacer on the sidewall of the opening, wherein the tops of the protective spacer are lower than the insulating layer;

forming a gate conducting layer in the opening;

removing the protective spacer and the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer;

implanting the exposed semiconductor substrate to form lightly doped drains;

forming a gate spacer to cover the gate conducting layer;

removing the etch stop layer and the pad layer to expose portions of the semiconductor substrate; and

implanting the exposed semiconductor substrate to form source/drain.

Claim 2 (original): The damascene gate process of claim 1, wherein the pad layer is an oxide layer.

Claim 3 (original): The damascene gate process of claim 1, wherein the etch stop layer is a nitride layer.

Claim 4 (original): The damascene gate process of claim 1, wherein the insulating layer is a tetraethylorthosilane layer.

Claim 5 (original): The damascene gate process of claim 1, wherein the protective spacer are nitride layers.

Claim 6 (original): The damascene gate process of claim 1, wherein the gate conducting layer is a laminated construction with two conducting layers.

Claim 7 (original): The damascene gate process of claim 6, wherein the conducting layer is a poly layer, a SiW layer, a W layer, or a silicide layer.

Claim 8 (original): The damascene gate process of claim 1, wherein the gate spacer is a nitride layer.

Claim 9 (original): The damascene gate process of claim 1, before the step of forming the gate conducting layer, further comprising a step of forming a gate oxide layer on the exposed semiconductor substrate of the bottom opening.

Claim 10 (original): The damascene gate process of claim 1, wherein the insulating layer is removed by HF or BHF.

Claim 11 (original): A damascene gate process, comprising:

providing a semiconductor substrate having a plurality of shallow trench isolation (STI) structures, an STI protective layer is formed on each of the STI structures;

sequentially forming a pad layer and an etch stop layer between the STI structures;

forming an insulating layer to cover the STI structures and the etch stop layer;

forming an opening between the structures by partially removing the insulating layer, the etch stop layer, and the pad layer;

forming a protective spacer on the sidewall of the opening, wherein the tops of the protective spacer are lower than the insulating layer;

forming dissimilar conducting layers acting as gate conducting layer in the bottom of the opening;

removing the protective spacer and the insulating layer to expose a portion of the semiconductor substrate and the etch stop layer;

implanting the exposed semiconductor substrate to form lightly doped drains beside the gate conducting layer;

forming a gate spacer to cover the gate conducting layer;

removing the etch stop layer and the pad layer; and

implanting the exposed semiconductor substrate to form source/drain.

Claim 12 (original): The damascene gate process of claim 11, wherein the STI structures are oxide layers.

Claim 13 (original): The damascene gate process of claim 11, wherein the STI protective layer is a nitride layer.

Claim 14 (original): The damascene gate process of claim 11, wherein the etch stop layer is a nitride layer.

Claim 15 (original): The damascene gate process of claim 11, wherein the insulating layer is a tetraethylorthosilane layer.

Claim 16 (original): The damascene gate process of claim 11, wherein the protective spacer is a nitride layer.

Claim 17 (original): The damascene gate process of claim 11, wherein the gate spacer is a nitride layer.

Claim 18 (original): The damascene gate process of claim 11, wherein the gate conducting layer is a laminated construction with two conducting layers.

Claim 19 (original): The damascene gate process of claim 18, wherein the conducting layer is a poly layer, a SiW layer, a W layer, or a silicide layer.

Claim 20 (original): The damascene gate process of claim 11, before the step of forming the gate conducting layer, further comprising a step of forming a gate oxide layer on the exposed semiconductor substrate of the bottom opening.

Claim 21 (currently amended): The damascene gate process of claim [[1]] 11, wherein the insulating layer is removed by HF or BHF.

Claim 22 (original): The damascene gate process of claim 11, wherein the pad layer is an oxide layer.